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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,517	12/11/2003	Gernot Eckstein	S0193.0011	1592

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DICKSTEIN SHAPIRO LLP
1177 AVENUE OF THE AMERICAS (6TH AVENUE)
NEW YORK, NY 10036-2714

EXAMINER	
JOHNSON, CARLTON	
ART UNIT	**PAPER NUMBER**
2136	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/735,517	ECKSTEIN ET AL.	
	Examiner	Art Unit	
	Carlton V. Johnson	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responding to application papers filed on **5-17-2007**.

2. Claims **1 - 10** are pending. Claims **9 - 10** are new. Claims **1, 3** are independent.

Response to Remarks

3. The following is in response to papers dated 5-17-2007. Applicant's arguments have thus been fully analyzed and considered but they are not persuasive.

3.1 Applicant argues, asynchronous circuit and clock based time variations. (see Remarks Pages 4, 5)

The Kash prior art discloses all claimed actions that must be taken from an external observation standpoint of an integrated circuit in order to defeat attempts to discover the internal operation(s) of the integrated circuit. (see Kash col. 7, lines 37-44: IC (integrated circuit); col. 3, line 66 - col. 4, line 3; col. 4, lines 8-13: time varying electrical (i.e. voltage supply) changes, prevent external detection of IC operation) By definition, an asynchronous circuit is disclosed whereby processing of the circuit is not directly correlated to a time-periodic event, such as a clock. (see Specification Page 2, Lines 5-8) Therefore, an asynchronous integrated circuit is an integrated circuit that operates in an asynchronous manner. This disclosure is within the description of the related art section of the Applicant specification and is considered appropriate for any asynchronous type operating integrated circuit. The Klughart prior art discloses an

integrated circuit that operates in an asynchronous manner, which is equivalent to applicant's invention. (see Klughart col. 16, lines 49-53: IC circuit; col. 37, lines 30-35: asynchronous operation) This equivalent operation discloses an integrated circuit that performs operations including required operations (such as voltage fluctuations, led fluctuations) intended to deceive external observation attempts to discover IC circuit operations.

3.2 Applicant argues, varying supply voltage. (see Remarks Page 5)

The Kash and Klughart prior art combination discloses the modification of a power supply voltage utilizing asynchronous operations. (see Klughart col. 22, lines 26-30; col. 37, lines 30-33: supply voltage modulated (regulated, modified))

3.3 The examiner has considered applicant's remarks concerning an asynchronous operating integrated circuit, whereby the random variation of the supply voltage causes a time jitter in the processing of the individual operations within the circuit, and any attempts to discover the synchronizing of individual measurements in such side channel attacks are successfully prevented. Applicant's arguments have thus been fully analyzed and considered but they are not persuasive.

Applicant's invention is the implementation of external intrusion detection procedures for integrated circuits utilizing asynchronous operations, which are not correlated to the timings of a clock. The Kash prior art discloses the IC procedures to detect and defeat external observation intrusion techniques. The Kash and Klughart

prior art combination discloses the additional limitation of asynchronous operations for the aforementioned integrated circuit. (see Klughart col. 16, lines 49-52: IC circuit; col. 22, lines 26-30; col. 37, lines 30-33: power regulate (power supply modification); col. 34, lines 42-48: protect from reverse engineering)

After an additional analysis of the applicant's invention, remarks, and a search of the available prior art, it was determined that the current set of prior art consisting of Kash (6,515,304) and Klughart (6,396,137) disclose the applicant's invention including disclosures in Remarks dated May 15, 2007.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims **1 - 5, 8** are rejected under 35 U.S.C. 102(e) as being anticipated by **Kash et al.** (US Patent No. **6,515,304**).

Regarding Claim 1, Kash discloses a method of preventing the external detection of operations in a digital integrated circuit (see Kash col. 7, lines 37-44: IC (integrated

circuit)) comprising an asynchronous circuit, comprising the method step of time-varying a supply voltage of said asynchronous circuit to time-shift the execution time of operations within said asynchronous circuit. (see Kash col. 3, line 66 - col. 4, line 3; col. 4, lines 8-13: time varying electrical (i.e. voltage supply) changes, prevent external detection of IC operation)

Regarding Claim 2, Kash discloses the method according to claim 1, wherein the time variation of said supply voltage takes place in a random way. (see Kash col. 8, lines 28-37: random generator utilized to vary voltage)

Regarding Claim 3, Kash discloses a digital integrated circuit comprising: an asynchronous circuit, and means for time-varying a supply voltage of said asynchronous circuit to time-shift the execution point of operations within said asynchronous circuit. (see Kash col. 3, line 66 - col. 4, line 3; col. 4, lines 8-13: time varying, voltage; col. 8, lines 28-37: operations on IC are time shifted (i.e. randomized))

Regarding Claim 4, Kash discloses the digital integrated circuit according to claim 3, wherein said means for time-varying said supply voltage comprises a random number generator. (see Kash col. 8, lines 28-37: random number generator; col. 8, lines 55-59: randomized delay)

Regarding Claim 5, Kash discloses the digital integrated circuit according to claim 4,

wherein said means for time-varying said supply voltage further comprises a noise voltage source driving said random-number generator. (see Kash col. 9, lines 42-45: noise utilized to prevent external detection of IC operation)

Regarding Claim 8, Kash discloses the digital integrated circuit according to claim 3, wherein said asynchronous circuit is formed for executing a coding algorithm. (see Kash col. 9, lines 20-23: smart card, programmable (i.e. coding algorithm) for IC (i.e. integrated circuit))

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims **6, 7, 9, 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kash et al.** as applied to claim **1** above, and further in view of **Klughart et al.** (US Patent No. **6,396,137**).

Regarding Claim 6, Kash discloses the digital integrated circuit according to claim 4, wherein said means for time-varying said supply voltage by said random-number generator. (see Kash col. 3, line 66 - col. 4, line 3; col. 4, lines 8-13: time varying electrical (i.e. voltage supply) changes; col. 8, lines 28-37: random generator utilize to

vary voltage) Kash does not specifically disclose a voltage regulator. However, Klughart discloses wherein said supply voltage further comprises a digital-analog converter transforming the digital values into an analog voltage. (see Klughart col. 34, lines 42-48; col. 34, lines 52-56: prevent reverse engineering for IC; col. 9, lines 13-16; col. 36, lines 12-15: analog/digital capabilities)

It would have been obvious to one of ordinary skill in the art to modify Kash as taught by Klughart to enable the capability to utilized analog/digital power conversion. One of ordinary skill in the art would have been motivated to employ the teachings of Klughart in order to enable the capability for the utilization of protective layers to prevent reverse engineering of investments in integrated circuit technology. (see Klughart col. 34, lines 49-56: " ... *The present invention requires that the foundation integrated circuit be covered with the regulator/switch function as implemented with a separate set of metal and semiconductor layers. This coverage of the lower foundation integrated circuit makes visual reverse engineering of the foundation integrated circuit exceedingly difficult, and completely prohibits probing of the active foundation integrated circuit.* ... ")

Regarding Claim 7, Kash discloses the digital integrated circuit according to claim 3, wherein said means for time-varying said supply voltage. (see Kash col. 3, line 66 - col. 4, line 3; col. 4, lines 8-13: time varying electrical (i.e. voltage supply) changes; col. 8, lines 28-37: random generator utilize to vary voltage) Kash does not specifically disclose a voltage regulator. However, Klughart discloses wherein said supply voltage further comprises a voltage regulator. (see Klughart col. 34, lines 42-48; col. 34, lines

52-56: prevent reverse engineering for IC; col. 22, lines 45-53; col. 27, lines 57-60; col. 23, lines 23-33: voltage regulator)

It would have been obvious to one of ordinary skill in the art to modify Kash as taught by Klughart to enable the capability for the usage of a voltage regulator. One of ordinary skill in the art would have been motivated to employ the teachings of Klughart in order to enable the capability for the utilization of protective layers to prevent reverse engineering of investments in integrated circuit technology. (see Klughart col. 34, lines 49-56)

Regarding Claim 9, Kash discloses the method according to claim 1. Kash does not specifically disclose whereby performs processing without correlation to a clock. However, Klughart, in the same field of endeavor, discloses wherein the asynchronous circuit is a type, which performs processing without correlation to a clock. (see Klughart col. 16, lines 49-52: IC circuit; col. 37, lines 30-35: performs asynchronous type operations, performs operations not directly correlated to a time-periodic event, such as a clock; col. 22, lines 26-30; col. 37, lines 30-33: power regulate (power supply modification))

It would have been obvious to one of ordinary skill in the art to modify Kash as taught by Klughart to enable the capability to perform asynchronous operations with an IC circuit. One of ordinary skill in the art would have been motivated to employ the teachings of Klughart in order to enable the capability for the utilization of protective layers to prevent reverse engineering of investments in integrated circuit technology.

(see Klughart col. 34, lines 49-56)

Regarding Claim 10, Kash discloses the digital integrated circuit according to claim 3. Kash does not specifically disclose whereby performs processing without correlation to a clock. However, Klughart, in the same field of endeavor, discloses wherein the asynchronous circuit is a type, which performs processing without correlation to a clock. (see Klughart col. 16, lines 49-52: IC circuit; col. 37, lines 30-35: performs asynchronous type operations, performs operations not directly correlated to a time-periodic event, such as a clock; col. 22, lines 26-30; col. 37, lines 30-33: power regulate (power supply modification))

It would have been obvious to one of ordinary skill in the art to modify Kash as taught by Klughart to enable the capability to perform asynchronous operations with an IC circuit. One of ordinary skill in the art would have been motivated to employ the teachings of Klughart in order to enable the capability for the utilization of protective layers to prevent reverse engineering of investments in integrated circuit technology. (see Klughart col. 34, lines 49-56)

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carlton V. Johnson whose telephone number is 571-270-1032. The examiner can normally be reached on Monday thru Friday , 8:00 - 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser Moazzami can be reached on 571-272-4195. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Carlton V. Johnson
Examiner
Art Unit 2136

NASSER MOAZZAMI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

7/19/07

C.J.
CVJ
July 9, 2007